TRF1216EVM

Contents

1 Introduction 1
2 EVM Test Configuration 2
3 Basic Test Procedure 3
4 Optional Configurations 5
5 Physical Description 6

List of Figures

1 System Block Diagram 2
2 Test Setup Block Diagram 2
3 TRF1216EVM Performance 4
4 TRF1216 NF Performance 5
5 Top Layer 1 6
6 Ground Plane Layer 2 7
7 Power Plane Layer 3 7
8 Bottom Layer 4 8

List of Tables

1 TRF1216EVM BOM 8

1 Introduction

1.1 Overview

This user's guide covers the evaluation module (EVM) for the TRF1216, a receive LNA and down-converter with integrated amplifiers and AGC for use in a WiMAX system. The TRF1216 operates in the 3.3 GHz to 3.8 GHz band.

1.2 System Block Diagram

The basic radio system block diagram in Figure 1 demonstrates where the TRF216 fits in the overall transceiver. The red box highlights the TRF1216 device.

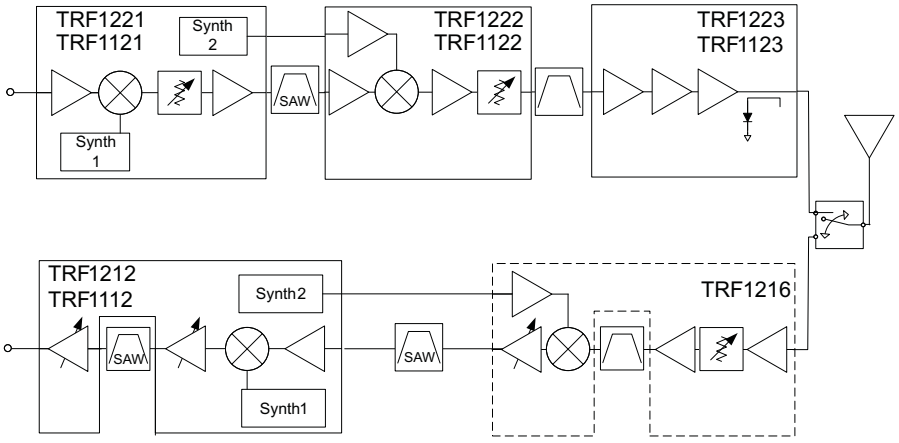


Figure 1. System Block Diagram

2 EVM Test Configuration

2.1 Test Block Diagram

The test setup for general testing of the TRF1216 is shown in Figure 2.

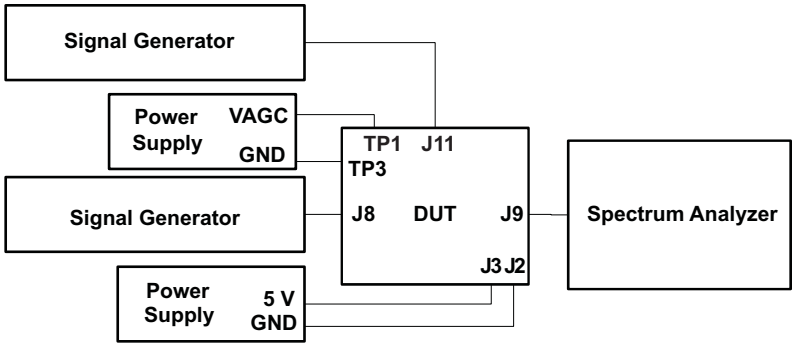


Figure 2. Test Setup Block Diagram

2.2 Test Equipment

The following equipment is required for completing RF Testing:

- Power supply with current readout (x2) — Agilent E3631 or equivalent
- Signal generator for input signal — Agilent E4438C or equivalent
- Signal generator for LO source — Agilent E4438C or equivalent
- Spectrum analyzer — Agilent E4440A or equivalent

2.3 Calibration

The output RF cable and input LO cable should be good-quality RF cables due to the high-frequency signals.

- Measure the insertion loss of the RF input cable at the frequency of operation. Compensate for the loss of this cable by incrementing the amplitude of the signal generator over the desired value by the amount of insertion loss. For example, if the insertion loss of the cable is 1.5 dB and the desired set-point is -45 dBm, the amplitude of the generator should be set to –43.5 dB.
- Measure the insertion loss of the RF cable used to inject an LO signal at the frequency of operation. Compensate for the loss of this cable by incrementing the amplitude of the signal generator over the desired value by the amount of insertion loss. For example, if the insertion loss of the cable is 1.2 dB and the desired set-point is 0 dBm, the amplitude of the generator should be set to 1.2 dB.
- Measure the insertion loss of the IF out cable at its frequency of operation. Compensate for the loss of this cable by adjusting the reference level offset in the spectrum analyzer.

3 Basic Test Procedure

This section outlines the basic test procedure for testing the EVM.

3.1 Initial Inspection

- Verify that the jumper connection at J5 is at the *5V_RX* location.
- Verify that the jumper connection at J6 is at the *Ext* location.

3.2 DC Test

- Connect +5V to J3; connect ground to J2.
- Engage power supplies.
- Verify that the current on is 175 ±25 mA.

3.3 Basic RF Test

- Inject a 3500-MHz CW signal in at J8 at –45 dBm; ensure that the RF output cable loss is compensated for.
- Connect the spectrum analyzer at J9.
- Set the spectrum analyzer center frequency to 456 MHz.
- Connect second power supply for AGC control to TP1: *AGCExt* and set to 1.5 V; ground can be connected at J2 or at TP3.
- Connect second signal generator at J11 and set to 0 dBm at frequency 3044 MHz; ensure that the LO cable loss is compensated for.
- Adjust AGC control for minimum gain by adjusting the AGC voltage to 1.5 V. The AGC voltage can be monitored at TP2 labelled *RF_AGC*.
- Measure the signal at 456 MHz and verify that the signal is at –30 dBm ±3 dB.
- Adjust AGC control for maximum gain by adjusting the AGC voltage to 0 V. The AGC voltage can be monitored at TP2 labelled *RF_AGC*.
- Measure the signal at 456 MHz, and verify that the signal is at –17 dBm ±3 dB.
- Change jumper at J5 to *GND* and verify that the signal decreases 10 ±2 dB.
- Revert jumper back to original position at *5V_RX*.

3.4 Modulated RF Performance

- Inject a 3500-MHz modulated signal in at J8 at –45 dBm.
- Set AGC voltage to 0 V for maximum gain.
- Inject the CW LO source at J11, and set to 0 dBm at frequency 3044 MHz. Note, this should be a low-phase noise source. Verify that the LO cable loss is compensated for.

- Connect a cable to the spectrum analyzer at J9 and initiate WiMAX analysis program.
- Set spectrum analyzer center frequency to: 456 MHz.
- Adjust reference level offset to appropriate range for output signal.
- Verify that the output signal power is at –18 ±2 dBm; ensure that the RF output cable loss is compensated for.
- Verify that the EVM performance is less than –40 dB; see Figure 3.

3.5 NF Performance

The noise figure of the evaluation board measured using a noise diode under maximum gain settings over frequency as shown in Figure 4.

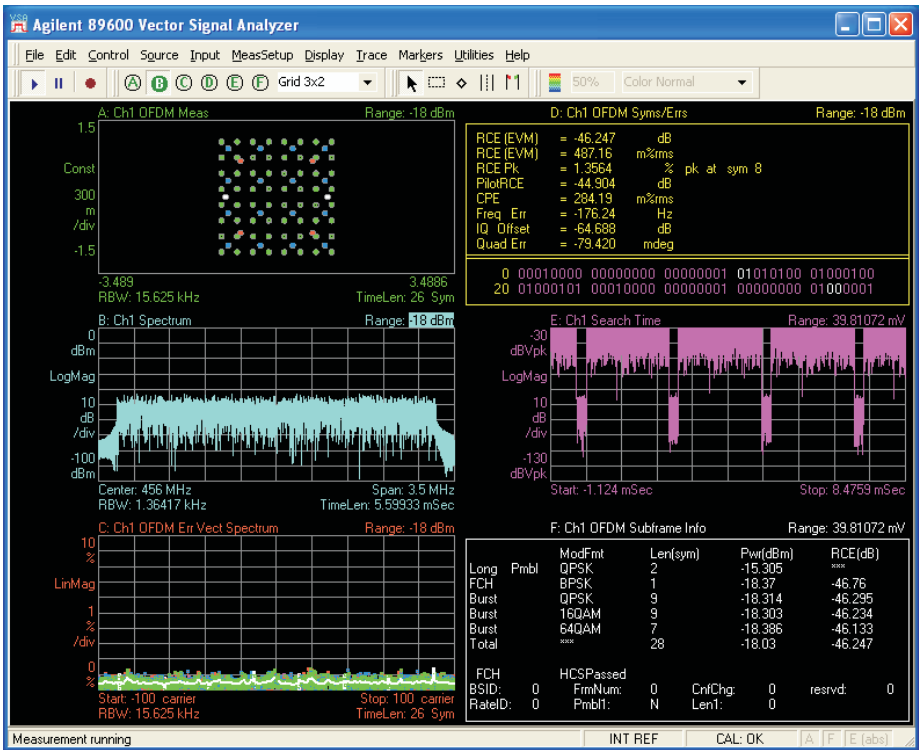


Figure 3. TRF1216EVM Performance

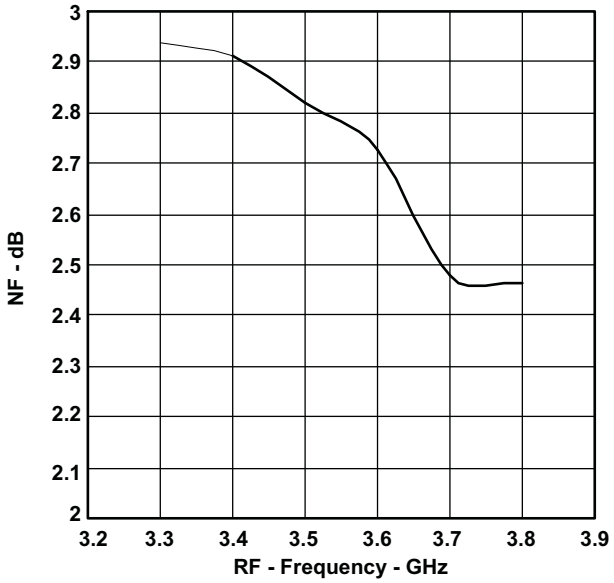


Figure 4. TRF1216 NF Performance

4 Optional Configurations

4.1 External RF Filter

The EVM is configured with the LNA output directly connected to the mixer input. These ports are intended to provide an option for an RF filter at this location. An external filter can be used by installing the jumpers to route the signal to SMA connectors. Note, this option also facilitates monitoring the LNA portion independent of the rest of the chip. To employ this option, the following modifications are required.

- Move R4 to R3 location.
- Move R8 to R9 location.
- Monitor at connectors J4 (LNA output) and J1 (mixer input).

4.2 Differential Inputs

The normal configuration uses transformers and baluns to convert the differential signals into single-ended to facilitate laboratory testing. Any of the inputs can be converted to differential operation which may be desirable when cascading one or more of the chipset's EVMs together.

4.2.1 IF Output

- Remove T1.
- Place R14: 0-Ω resistor (1210)
- Place R10: 0-Ω resistor
- Differential outputs at J9 and J7

4.2.2 LO Input

- Remove T2.
- Jumper across pads of T2 (input to output on each side) using a 0-Ω 0201 resistor
- Place 3.6-pF capacitor at R15.
- Differential inputs at J10 and J11

4.3 Internal AGC Control

The AGC control can be driven internally by adjusting the resistor potentiometer at R1. To employ this option, move the jumper at J9 to “Int” and adjust the AGC voltage by tuning the potentiometer at R1 between 0 V and 1.5 V.

5 Physical Description

This section describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

5.1 PCB Layout

The EVM is constructed on a 4-layer, 2.5-inch × 2.5-inch, 0.062-inch thick PCB using FR4-170 material. Figure 5 through Figure 8 show the PCB layout for the EVM.

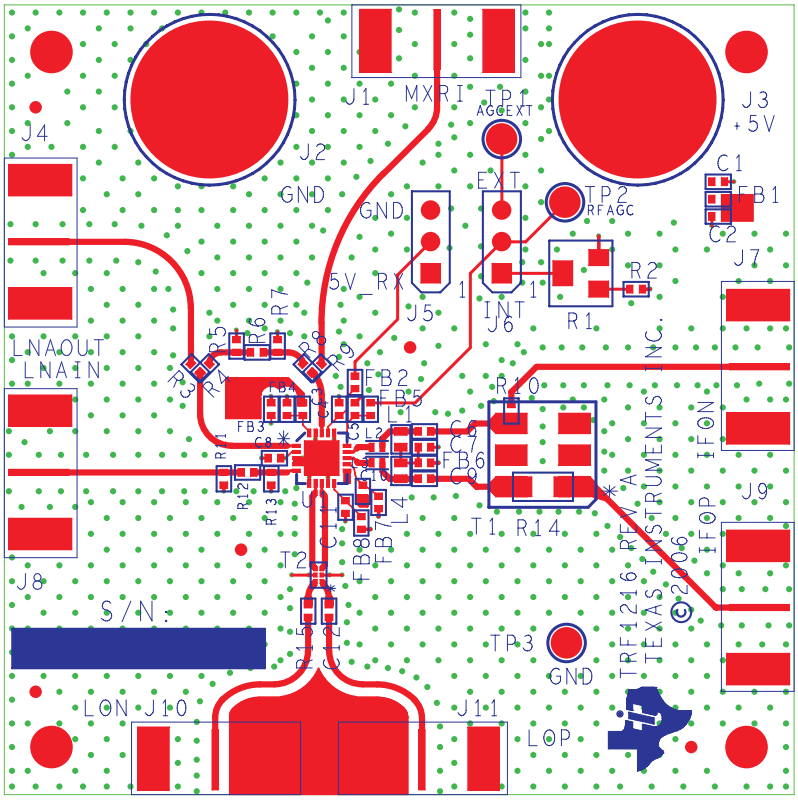


Figure 5. Top Layer 1

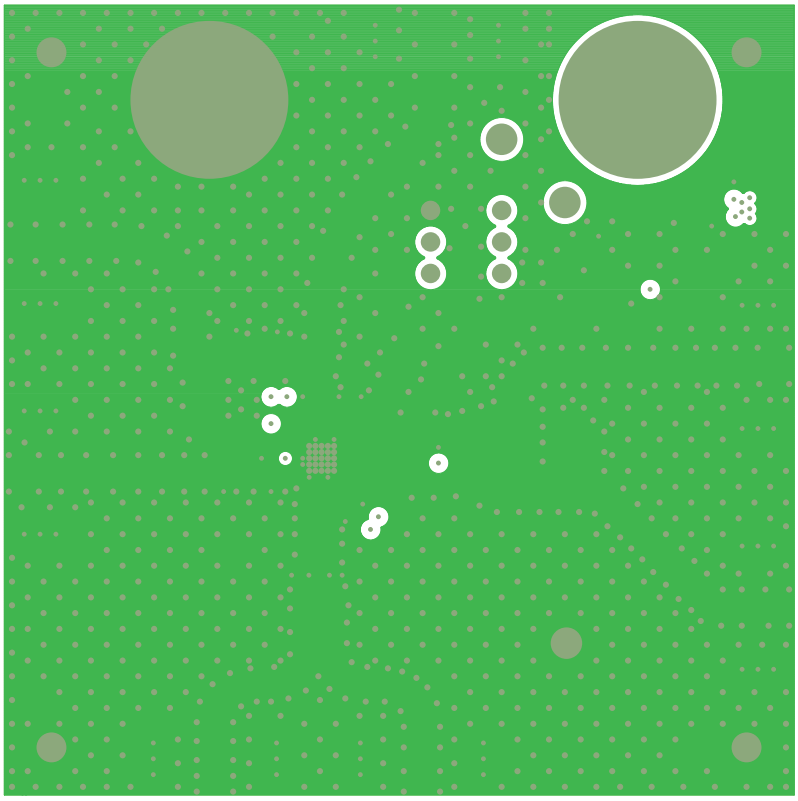


Figure 6. Ground Plane Layer 2

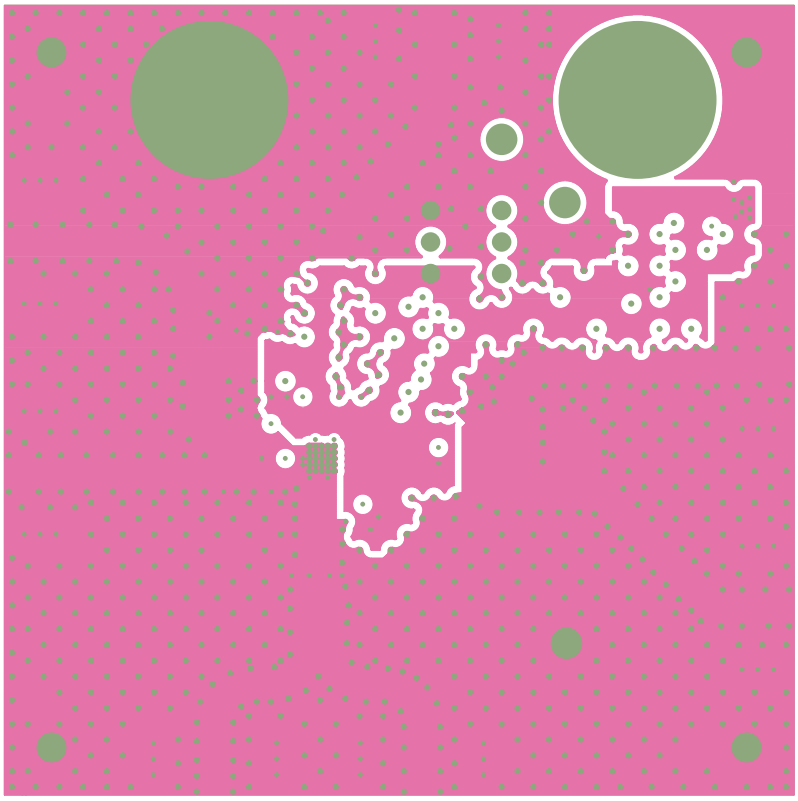


Figure 7. Power Plane Layer 3

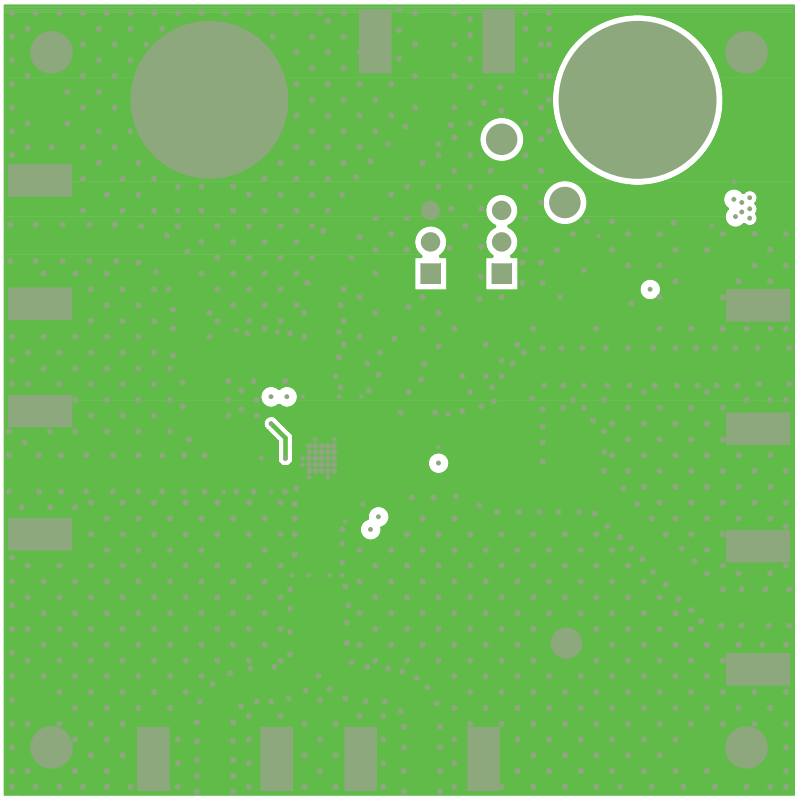


Figure 8. Bottom Layer 4

5.2 Parts List

Table 1 lists the parts used in constructing the EVM.

Table 1. TRF1216EVM BOM

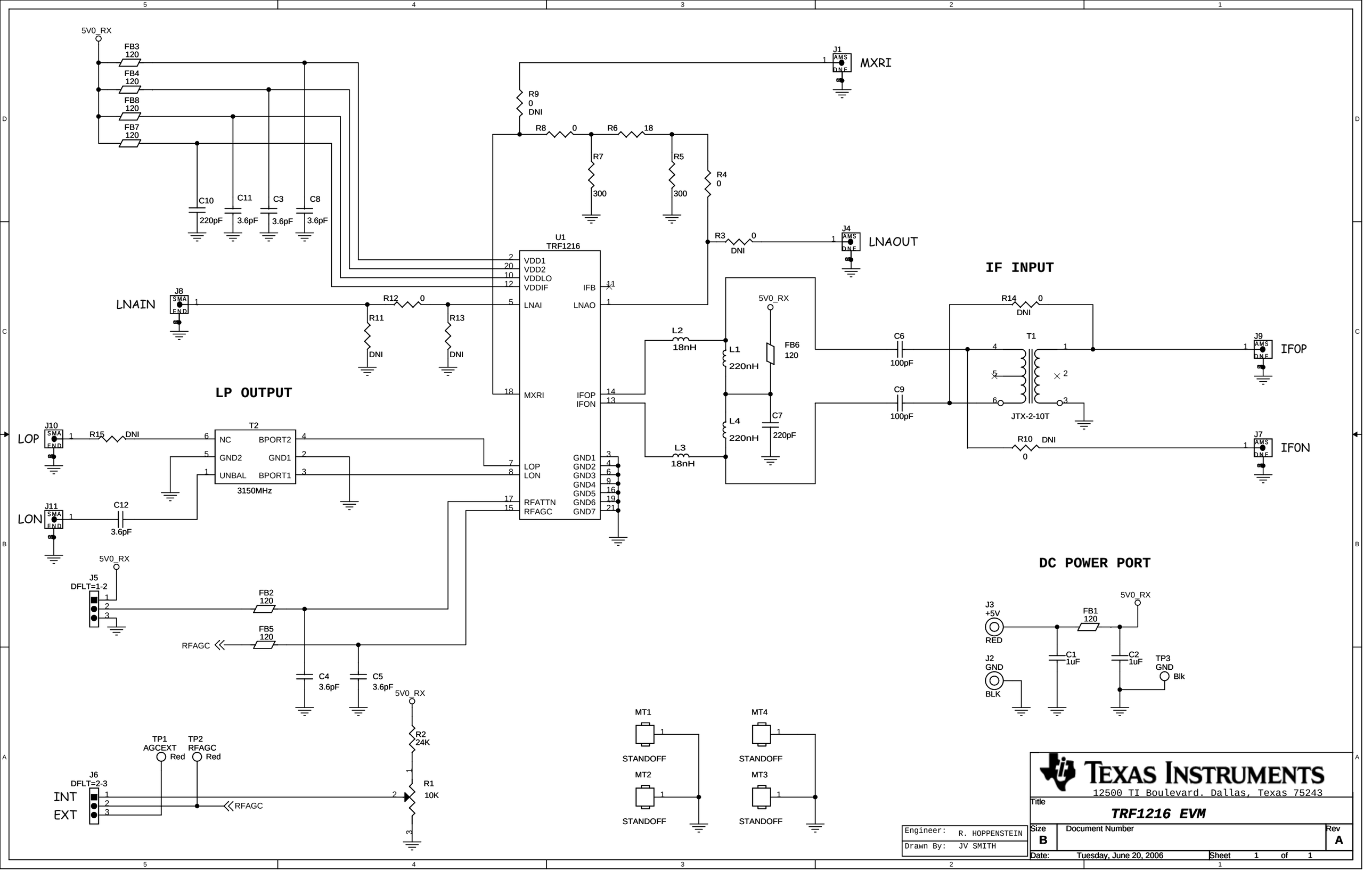
QTY	Reference	Value	Mfr_Name	Part Number	Note
2	C1 C2	1µF	Panasonic	ECJ-0EB1A105M	
6	C3 C4 C5 C8 C11 C12	3.6pF	Murata	GRM1555C1H3R6CZ01D	
2	C6 C9	100pF	AVX	04025A101JAT2A	
2	C7 C10	220pF	Murata	GRM1555C1H221JA01D	
8	FB1 FB2 FB3 FB4 FB5 FB6 FB7 FB8	120	Murata	BLM15AG121SNIB	
7	J1 J4 J7 J8 J9 J10 J11	SMA_END_FLAT	Johnson Components	142-0701-851	
1	J2	BLK	ALLIED ELECTRONICS	ST-351B	
1	J3	RED	ALLIED ELECTRONICS	ST-351A	
2	J5 J6	Header_1x3_100	SAMTEC	TSW-103-07-L-S	
2	L1 L4	220nH	Coilcraft	0603CS-R22XJLU	
2	L2 L3	18nH	Coilcraft	0402CS-18NXJLU	
4	MT1 MT2 MT3 MT4	STANDOFF	KEYSTONE	1902CK	STANDOFF
1	R1	10K	Bourns	3214W-1-103E	
1	R2	24K	Panasonic	ERJ-2GEJ243X	
3	R3 R9 R10	0	Panasonic	ERJ-2GE0R00X	DNI
3	R4 R8 R12	0	Panasonic	ERJ-2GE0R00X	
2	R5 R7	300	Panasonic	ERJ-2GEJ301X	

Table 1. TRF1216EVM BOM (continued)

QTY	Reference	Value	Mfr_Name	Part Number	Note
1	R6	18	Panasonic	ERJ-2GEJ180X	
3	R11 R13 R15	DNI	Panasonic	DNI	DNI
1	R14	0	Panasonic	ERJ-8GEY0R00V	DNI
1	T1	JTX-2-10T	Minicircuits	JTX-2-10T	
1	T2	3150MHz	Anaren	BD3150L50200A00	
2	TP1 TP2	Red	Keystone	5000	
1	TP3	Blk	Keystone	5001	
1	U1	TRF1216	TI	TRF1216	

5.3 Schematic Drawing

The schematic drawing follows this page.



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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 5 V and the output voltage range of 0 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85° C. The EVM is designed to operate properly with certain components above 85° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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